SUPER EFFECTS

The Synergistic Effects of TRIZ,

The Theory of Inventive Problem Solving

Gunter Ladewig, Founder, PRIMA Performance Ltd., info@primaperformance.com

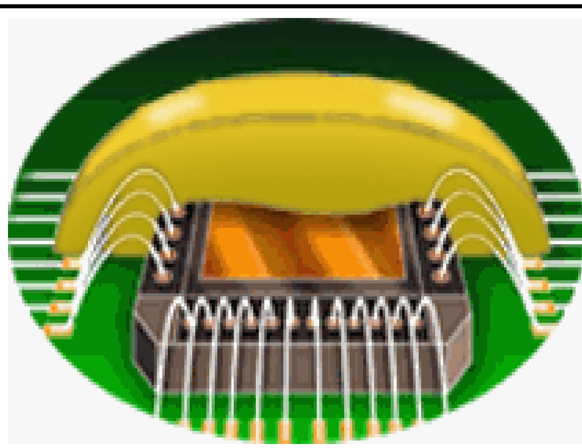
Robert Lyn, Microbonds Inc., CTO, rlyn@microbonds.com

Genrich Saulovich Altshuller (1926 – 1998), wondered, "Could inventions be the result of systematic inventive thinking?" Over half a century, Altshuller and his associates investigated some 200,000[1] patents. They found that exceptional patents improved the performance of a technological system through elimination of its fundamental constraint by resolving contradictory requirements, like increasing speed without higher fuel consumption. Altshuller discovered that as technological systems evolved to their next level of performance by resolving contradictory requirements, systems tended to progress along certain vectors or Trends of Evolution. Each vector of evolution had discrete phases, or performance levels, which define where a system was, where it is, and where it will be in its evolutionary journey. Another revelation was the frequent occurrence of a windfall of benefits, or super effects, which occurred when a system progressed from one phase to the next by eliminating its fundamental contradiction. Not only were many costly add-ons or processes, and expensive tolerances were no longer required, many systems had inherited valuable, new, product differentiating, capabilities and features. The result, TRIZ, a Russian acronym for The Theory of Inventive Problem Solving, provides us with a methodology for systematic creativity.

Background: The increasing and never ending demand for more function from electronic devices in smaller form factors continues to accelerate and force pressure upon electronics systems to meet these requirements. To satisfy these demands, designs must be optimized in order to remove the critical roadblocks to attaining maximum performance at minimal cost. An increasing amount of attention, which has traditionally been focused on semiconductor chip developments and systems design, is now being directed towards the most severe system performance constraint, i.e. the interconnection technologies used to join these components together. A new strategic interconnection technology, called X-Wire™, Insulated Wire Bonding Technology, developed by Microbonds Inc., is poised to remove the fundamental constraint that currently impedes the economic viability of next-generation, high performance designs. This paper describes the chain reaction of benefits, referred to by TRIZ as super effects, which occur when wire-bonding with X-Wire™.

Current Wire Bonding Technology: Wire bonding is the process of welding a fine conductive wire (usually Gold), approximately half the diameter (25 microns) of a human's hair, from an IC, integrated circuit, chip interconnection pad to a substrate pad as shown in Exhibit 1. It is used in over 90 percent of all world wide IC packages.

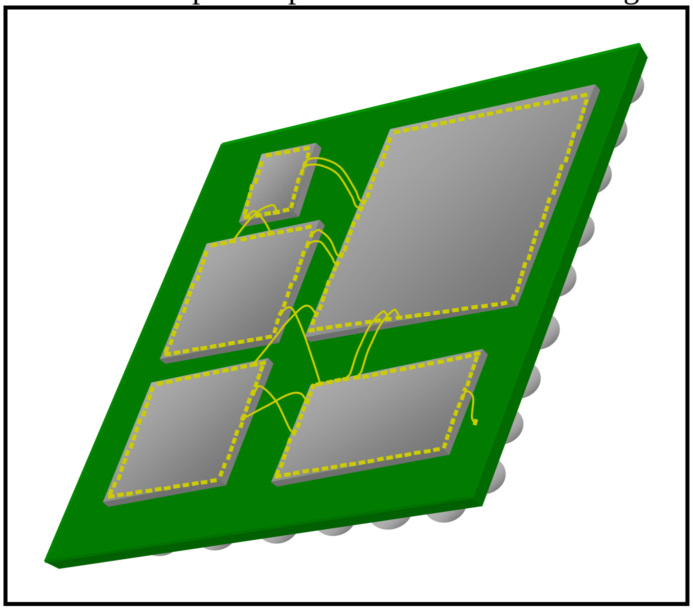
Exhibit 1: Wire bonding, chip to pad interconnection



SOURCE: Loctite

Since total system performance is most severely limited by the length of chip to chip interconnecting wire (Exhibit 2), requiring designers to minimize the number of chips used.

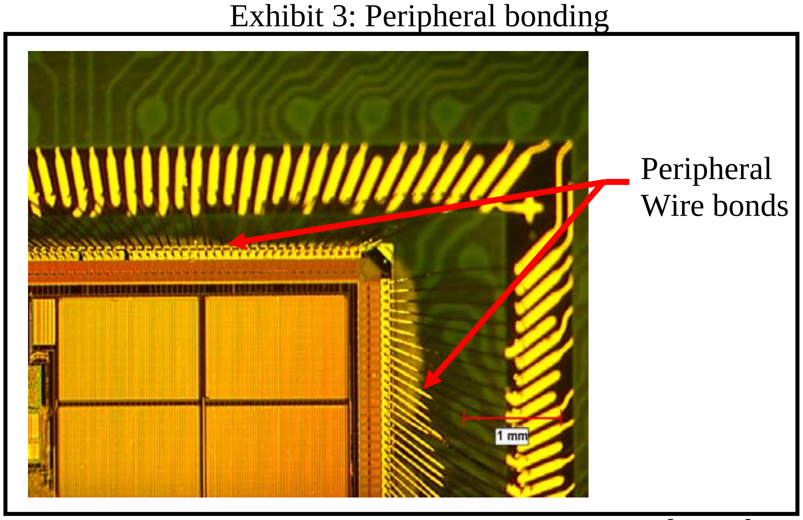
Exhibit 2: Chip to chip interconnection wire length



SOURCE: The authors

This constraint forces the designer into a trade-off contradiction, whereby wires should be close, ideally touch, to maximize I/O, input/outputs per chip, and the wires should be far apart to prevent electrical shorts. The wire bonding industry's answer to this dilemma was to space out wires by only bonding around the chip's perimeter (Exhibit 3), thus resulting in decreased performance (low I/O per chip) and wasted expensive 'real estate' at the centre of the chip.

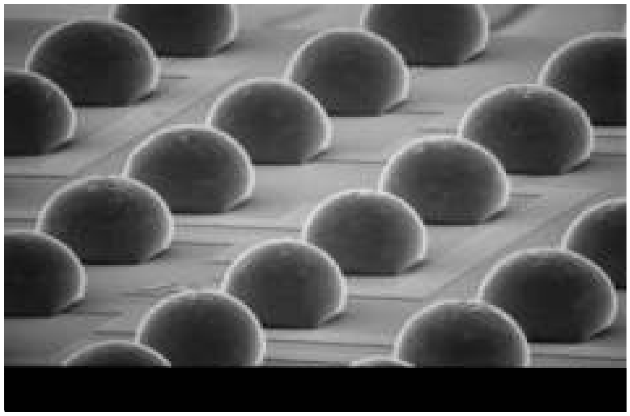
Exhibit 3: Peripheral bonding



SOURCE: The authors

Because industry never solved this fundamental issue and due to the ever increasing demand for more performance (I/O per chip), other but very expensive new technologies with area array capability such as Area Array Flip Chip were developed. (Exhibit 4)

Exhibit 4: Area array, Flip Chip

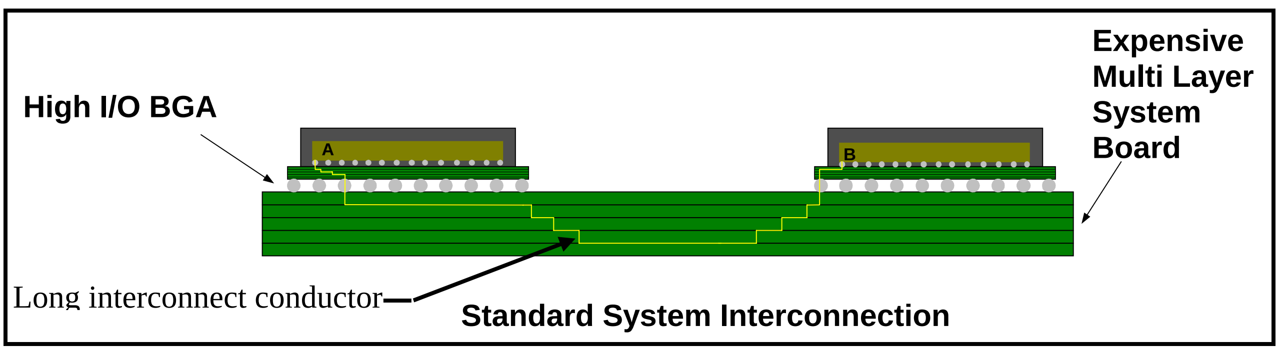


Area array of solder balls for Silicon chip to substrate interconnection

SOURCE: The authors

Although flip chip provides some performance improvement, the unresolved interconnect wiring problem was never eliminated and merely transferred to expensive, multi-layer substrates with long layer to layer connecting conductors. (Exhibit 5)

Exhibit 5: Multi-layer interconnect substrates



SOURCE: The authors

TRIZ and The Trends of Evolution: As mentioned previously, Altshuller discovered that technological systems improve their performance, i.e. eliminate constraints, by evolving from one phase to the next along predictable ‘vectors’ of evolution (‘Back to the future’). We can perform a ‘medical’ on any technological system by determining which ‘vectors’ are involved and what the system’s maturity is subject to the phase locations along various vectors. In other words, we can perform an innovation potential assessment on any system to determine its opportunities for improvement. We can determine if the system has ‘headroom’ for improvement (more phases to exploit) with the current technology, or if it is bumping its head at the end of a vector and for this reason must change to a brand new technology (new vector), or if an evolutionary phase has been skipped, enabling us to go back to that phase, exploit it, and thus ‘hollow-out’ the competition that has committed itself to a more expensive process and or infra-structure.

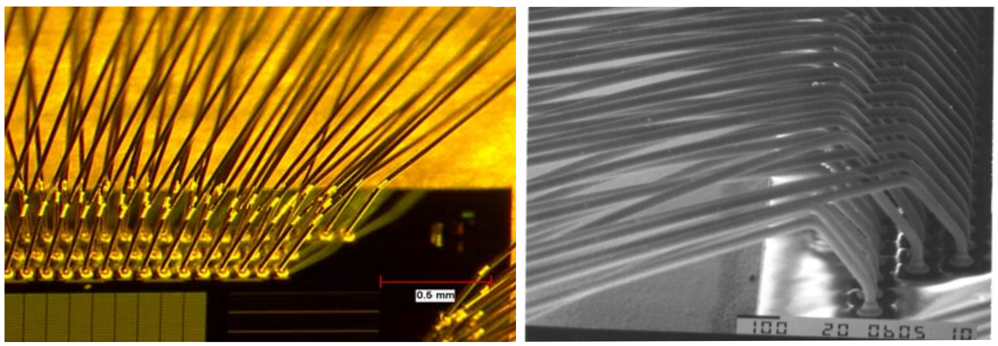
Subject to how the Trends of Evolution are grouped, there are in excess of 30 trends. The trend that applies to our most fundamental IC constraint, chip to chip interconnect wire length, or chip ‘wireability’, is the Trend of Geometric Evolution for a Line. Generally speaking geometric structures tend to evolve from a single point towards complex three dimensional structures as follows:

Point → Line → 2D Lines (planar) or curves → 3D Lines (cubic) or Curves → 3D Complex Curves. If we use sewing as an example, the first phase would be a single stitch, then a straight line of stitched thread, then a plane of woven or stitched fabric, next three dimensionally, interconnected layers of fabric, then three dimensionally interconnect complex structures.

Review of Exhibits 1 to 3 reveals that phase 3, 2D lines in a planar arrangement was only partially completed. Because the contradiction of having wires touch to maximize the number of wires and at the same time have wires that are far apart to prevent electrical shorting was never solved, only peripheral chip bonding was used to maximize wire spacing, thus leaving the whole centre of the chip completely empty. Or, if performance demands couldn’t be satisfied by wire bonding, then expensive new technologies like Flip Chip were adopted (Exhibit 4 and 5). Microbonds Inc. exploited this opportunity of a skipped phase of evolution with their development of X-Wire™.

X-Wires™ touch without shorting: Microbonds Inc. solved this contradiction by developing a one micron-thin, bond wire insulating material that has the ability to be used on standard wire bonding assembly equipment. With this technology the whole area of the chip, including its center, could now be wire bonded (See Exhibit 6), thus requiring fewer chips resulting in improved total system performance due to fewer and shorter inter-chip wire connections.

Exhibit: 6



SOURCE: The authors

Numerous obstacles had to be overcome. To name a few, the coating: 1 – Had to be thin, yet have high dielectric strength, 2 – Must have high flexural strength but crack resistant, (See Exhibit: 7) 3 – Must not inhibit bonding, 4 – Must be non-contaminating (leaving no residue on equipment), 4 – Solvent resistant, 5 – Adhere to Gold, and 6 – Temperature stable up to 250°.

Exhibit: 7

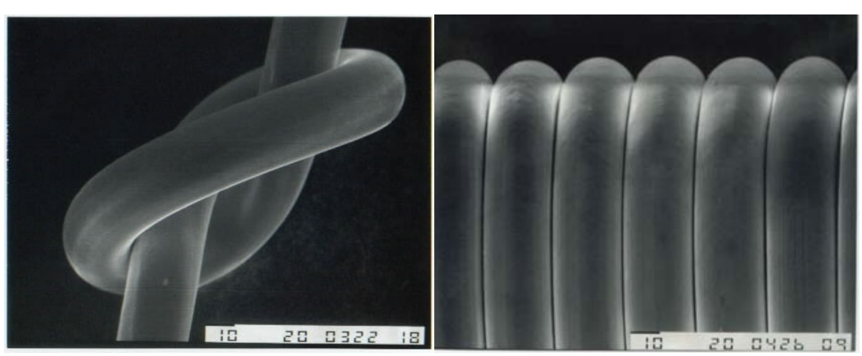


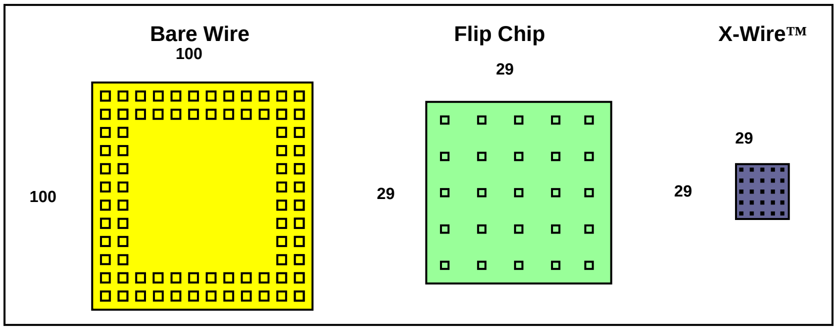
Fig. 1: (0.5 mil radius) **Fig. 2: (2.5 mil radius)**

SOURCE: The authors

A chain reaction of super effects: Is poised to have a global impact on the electronics industry due to the implementation of X-Wire™. To name a few, these are:

1. Increased total system performance due to fine pitch, high I/O per chip capability,
2. Relaxed design specifications due to increased process robustness and improved performance,
3. Lower substrate cost due to increased connectivity,
4. Reduced die size resulting in potential billion dollar savings due to increased wafer yields, (See Exhibit: 8)

Exhibit: 8



SOURCE: The Authors

5. X-Wire™ is a 'plug and play' technology that enables next generation products with the current world-wide wire bonding infra-structure,
6. Quick response engineering changes can be implemented to correct design errors by wiring directly from the bond pad to the substrate pad without worrying about wire shorting, regardless of location, routing complexity, or length of wire,
7. It's an enabling technology for system in a chip, SiP, and stacked die assembly. Because X-Wires don't short, they can be tightly spaced for high I/O, input/output, systems in a chip or for stacked die assemblies,
8. Increased manufacturing quality and product reliability due to immunity from wires shorting during the bonding process or during molding when the chip is encapsulated with plastic, and finally and most importantly
9. Savings resulting from all of the above benefits.

To summarize: The above article is a summary of a windfall of benefits that was achieved when a technological system's fundamental constraint or contradiction was solved. We illustrated how just one Trend of Evolution, there are more than thirty trends, could be used as a competitive weapon. Trends not only tell us where our products are on their evolutionary journey versus lets say a competitor's product, but also where products must evolve to, and perhaps most importantly, they show us opportunities for improvement, or as in our case, how to hollow-out the competition when an evolutionary phase has been skipped. TRIZ however has many more application and tools than what was shown with The Trends of Geometric Evolution of a Line. TRIZ provides us with a methodology, distilled from the real world of the world-wide patent base, for the creation of world class products and processes that's based on the best tools used by the best inventors for the creation of their best ideas.

Gunter Ladewig is founder of PRIMA Performance Ltd.

Endnotes:

[1] *Systematic Innovation Using TRIZ,* CREAX Press, Belgium, 2002

Garasomov, V. M., Litvin, S.S. *'Basic Statements of the Technique for Performing VEA. Convolution and Super effects'* Journal of TRIZ, 3, 2/92, pp. 7-45 (in Russian)

Savransky, S. D. *'ENGINEERING OF CREATIVITY, Introduction to TRIZ Methodology of Inventive Problem Solving'* CRC Press, 2000

Tummala, R. R. *'Fundamentals of Micro System Packaging'* McGraw-Hill, 2001

Tummala R. R. *'Microelectronics Packaging Handbook'* Van Nostrand Reinhold, 1989

Harman G. H. *'WIRE BONDING IN MICROELECTRONICS'* The International Society for Hybrid Microelectronics, 1989.